Eligibility:

1) He/ she must be a faculty member in the Department of **Electronics and Communication Engineering / Electrical Engineering / Computer Science and Engineering /Instrumentation Engineering /Information Technology /Physics** with basic **VLSI** knowledge/ **Mathematics** with basic **VLSI** knowledge/ **Material Science** with basic **VLSI** knowledge/ related Departments and Centres.
2) B.E. / B. Tech. or equivalent degree holders in the above mentioned disciplines with minimum teaching experience of 2 years and moderate teaching experience in the area of Analog and Digital Circuits.
3) M.E / M.Tech. degree holders in the above mentioned disciplines with minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.
4) Ph.D. degree holders should have a minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.

Who may benefit:

The workshop is likely to benefit regular/visiting faculty colleagues who are teaching subjects like VLSI Design, Fundamentals of Radio Frequency Engineering, Design and Implementation of Mixed Signal Circuits and Systems, Design and Analysis of Radio Frequency Integrated Circuits, Mixed Signal and RFIC Design, Analog Front-End Design, Digital VLSI Circuits, VLSI Architecture for Video Processing, etc.

Note:

Please note that this ISTE STTP is conducted under the CEP IIT Kharagpur. Live recording of the course and other created contents will be released under Open Source through a portal. The recorded CD/DVD of the course lectures will be available for distribution, at cost, to any individual or institution. All participants are required to sign an undertaking for such release of contents contributed by them during and after the STTP. The recognition and citation will naturally be made for all contributors.

Course Fee:

This ISTE STTP on 'CMOS, Mixed Signal and Radio Frequency VLSI Design' is funded by the National Mission on Education through ICT (MHRD, Government of India), therefore there is no course fee for participation.

Accommodation:

Remote Centers are being funded to provide tea/lunch on each day of the workshop, and for accommodation, wherever available, for a limited number of outstation participants. **Travel expenses up to Rs. 1000/- one way and one-time will be reimbursed against proof of actual expenditure, for participants beyond a distances of 100 km from the remote center.**

How to Apply:

Those willing to attend this course should register online.

Online Registration link:

http://www.nmeict.iitkgp.ernet.in/vlsidmain.php

Address for Communication:

Admin Team,
Project "T10KT", IIT Kharagpur
Vikramshila Building, ground floor of Kalidas Auditorium
Kharagpur – 721302. West Bengal, India.

Contact Numbers:

Admin Team: +91 3222-281497
Account Team: +91 3222-281498
Moodle Team: +91 3222-281070
A-View Team: +91 3222-281072
Mobile Number: +91 8145226903

email: office_nmeict@iitkgp.ac.in
Website: http://www.nmeict.iitkgp.ernet.in

TWO-WEEK ISTE STTP ON CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN

National Mission on Education through ICT
(MHRD, Govt. of India)

30th January, 2017 to 4th February, 2017

Indian Institute of Technology
Kharagpur 721302
India

Introduction:

IIT Kharagpur and IIT Bombay are working together with Engineering Colleges of India to enhance the teaching skills of our faculty colleagues in core Engineering and Science subjects by conducting ISTE Short Term Training Programmes (STTPs) under Train Ten Thousand Teachers (T10KT) project using 353 established remote centers across India. Participating teachers attend live lectures at a remote center close to their own college, and also attend tutorial and lab sessions conducted in the same centers. The lecture transmission and live interaction takes place in distance mode using A-VIEW technology through Internet at the selected remote centers across the country.Since December 2009, a number of two-week ISTE STTPs were conducted on various Engineering subjects. We have reached out to more than 1,00,000 teachers and helped them to enhance their teaching skills in these subjects.

In order to run these STTP at selected remote centers, we invite expert faculty members from various remote centres to a five-day Coordinators' training programme held at IIT Kharagpur or at IIT Bombay, at least two months before the main STTP. The trained Coordinators then act as Workshop Coordinators during the main STTP liaising between the participants at their Remote Centers and IIT Kharagpur / IIT Bombay from where the interactive lectures are transmitted live. During the main STTP, the workshop Coordinator at every center supervises the tutorials and laboratories. All the lectures and tutorial sessions are recorded at IIT Kharagpur or at IIT Bombay. The final edited audio-visual contents, along with other course material are released under Open Source. The contents can be freely used later by all teachers, students and other learners.

In the backdrop of the success of these STTPs, we now announce another 6 day ISTE STTP on **"CMOS, Mixed Signal and Radio Frequency VLSI Design"** during January 30 - February 4, 2017 under **Blended MOOCs** (Massive Open Online Courses) model.

Here,

1. The participating teachers will complete the equivalent of two-week full time work online, spread over 6 physical weeks where video lectures and assignments will be uploaded beforehand.
2. After completing the online assignments spread over 4 to 5 weeks the participants will assemble at the selected Remote Centers for 6 days face to face interaction and lecture sessions through A-VIEW and will complete team assignments, tutorials, quizzes etc.
3. Offline assignments will be uploaded and the participants will have to complete these assignments within a stipulated time.
4. There will also be a system of students' feedback in the Main STTP.

The above proposed model is tentative and subjected to minor changes

Course Justification:

Design, analysis and implementation of CMOS Mixed Signal and RFIC are attractive topics both in academia and Industry. CMOS RFIC design is a challenging and critical engineering task particularly in the arena of deep sub-micron technology. There is a strong demand of manpower having thorough knowledge and hands on experiences in VLSI design using state of the art EDA tools. The course will focus on those issues along with case studies.

Course Domain:

Electronics Engineering/Electrical Engineering/Computer Science and Engineering

Expectation from the Participants:

It is assumed that before taking the courses, the participants are familiar with introduction to electronic circuit components, signal and system theory, VLSI design technology and basic CAD flow for electronic system.

Course Objective:

Design and implementation methodology of :

1. **Analog front end for sensor interface:** Instrumentation Amplifier (IA), chopper, Variable Gain Amplifier (VGA)
2. **Data converters:** SAR & pipelined ADC.
3. **Digital VLSI:** a) Static MOS gate circuits b) High-Speed CMOS Logic Design c) Transfer Gate and Dynamic Logic Design d) VLSI architectures for video processing
4. **RF circuits:** Introduction to RFIC design.
5. **Design and implementation of typical RF Tx-Rx sub-components:** (a) Low Noise Amplifier (LNA) (b) Mixer c) Frequency synthesizer (d) Power amplifier (e) Lay out and chip level integration

Design Methodology:

From pen-paper design of various mixed signal/RF circuit blocks to schematic level implementation and then sub-sequent physical design, post-layout synthesis and simulation.

Course Modules:

1. **Radio Frequency Integrated Circuits (RFIC) :**

   Module-A Fundamental of RFIC design, How RF design alters from traditional analog design. Various commercial protocols, basic Tx-Rx Architecture.

   Module-B Various performance parameters, Noise.

   Module C Design of LNA, VCO, Mixer and frequency synthesizer, Power amplifier, High speed I/O(SERDES), layout of RF circuit design.

2. **Mixed Signal Blocks :**

   i) Digital VLSI Design: High-Speed CMOS Logic, Transfer Gate and Dynamic Logic

      a) Basics of video processing

      b) VLSI Architectures for video processing

   ii) Analog Design: Analog front-end electronics (AFE), SAR ADC, Pipelined ADC.

Duration and Venue:

The duration of the STTP will be six working days. It will start on **Monday 30th January, 2017 at 9:30 AM** and will end on **Saturday 4th February, 2017**.The participants must report to the respective remote centres by 8:00 AM on 30th January, 2017.

Venue: 206 remote centers located in different parts of the country. The list of participating remote centers is given along with online application form.

Teaching Faculty:

1. Prof. T. K. Bhattacharya, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email: tkb@ece.iitkgp.ernet.in
2. Prof. Indrajit Chakrabarti, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email : indrajit@ece.iitkgp.ernet.in
3. Dr. Mrigank Sharad, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email : mrigank@ece.iitkgp.ernet.in

Get this letter printed on your Institute Letter Head

Date:

From,

_____ (Head of the Institute's Name)

_____ (Designation)

To,

The Project Co-ordinator

Project "T10KT", IIT Kharagpur

Vikramshila Building,

Ground floor, Kalidas Auditorium

IIT Kharagpur, Kharagpur – 721302

Permission letter for Two Week ISTE STTP on CMOS, Mixed Signal and Radio Frequency VLSI Design.

This is to certify that the following participants are regular teaching employees of of our Institute with one of the following designation :- (Jr. Lecturer/ Lecturer/Sr. Lecturer/Asst. Professor/Associate Professor/ Professor/HOD/ Reader/Vice- Principal/Visiting Faculty/ Teaching Fellow).

SL No.	Name	Designation	Department

The faculty members are allowed to attend the workshop on CMOS, Mixed Signal and Radio Frequency VLSI Design under the National Mission on Education through ICT (MHRD, Govt. of India) from dated 30/01/2017 to 04/02/2017 in the _____ (Remote Center Name with Remote Center ID).

The Institute has no objection to his/ her participation in the workshop. We would make sure that **no official duties** will be delegated which may affect his/ her participation, during workshop.

Thank You,

Institute Head's Signature with Stamp